Voltage Divider Bias

ENGI 242
ELEC 222

BJT Biasing 3
For the Voltage Divider Bias Configurations
• Draw Equivalent Input circuit
• Draw Equivalent Output circuit
• Write necessary KVL and KCL Equations
• Determine the Quiescent Operating Point
  – Graphical Solution using Load lines
  – Computational Analysis
• Design and test design using a computer simulation
Voltage Divider Input Circuit Approximate Analysis

This method is valid only if \( R_2 \leq \frac{1}{\beta} R_E \)

Under these conditions \( R_E \) does not significantly load \( R_2 \) and it may be ignored:

\( I_B \ll I_1 \) and \( I_2 \approx I_1 \)

Therefore:

\[ V_B = V_{CC} \left( \frac{R_2}{R_1 + R_2} \right) \]

We may apply KVL to the input, which gives us:

\[ -V_B + V_{BE} + I_E R_E = 0 \]

Solving for \( I_E \) we get:

\[ I_E = \frac{V_B - V_{BE}}{R_E} \]
**Input Circuit Exact Analysis**

This method is always valid must be used when $R_2 > 0.1 \beta R_E$

Perform Thevenin’s Theorem

Open the base lead of the transistor, and the Voltage Divider bias circuit is:

$$V_{TH} = V_{CC} \left( \frac{R_2}{R_1 + R_2} \right)$$

Calculate $R_{TH}$

We may apply KVL to the input, which gives us:

$$-V_{TH} + I_B R_{TH} + V_{BE} + I_E R_E = 0$$

Since $I_E = (\beta + 1) I_B$

$$-V_{TH} + I_E \frac{R_{TH}}{\beta + 1} + V_{BE} + I_E R_E = 0$$

Solving for $I_E$ we obtain:

$$I_E = \frac{V_{TH} - V_{BE}}{R_{TH} \left( \frac{\beta + 1}{\beta + 1} + R_E \right)}$$

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**Redrawing the input circuit for the network**
Determining $V_{TH}$

$$V_{TH} = V_{CC} \left( \frac{R_2}{R_1 + R_2} \right)$$

Determining $R_{TH}$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$
The Thévenin Equivalent Circuit

Note that $V_E = V_B - V_{BE}$ and $I_E = (\beta + 1)I_B$

Input Circuit Exact Analysis

We may apply KVL to the input, which gives us:

$-V_{TH} + I_B R_{TH} + V_{BE} + I_E R_E = 0$

Since $I_E = (\beta + 1)I_B$

$-V_{TH} + I_E \frac{R_{TH}}{\beta + 1} + V_{BE} + I_E R_E = 0$

Solving for $I_E$ we obtain:

$I_E = \frac{V_{TH} - V_{BE}}{\frac{R_{TH}}{\beta + 1} + R_E}$
Collector-Emitter Loop

\[ V_{CC} - I_C R_C + V_{CE} + I_E R_E = 0 \]

Assuming that \( I_E \cong I_C \) and solving for \( V_{CE} \):

\[ I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E} \]

Solve for \( V_E \):

\[ V_E = I_E R_E \]

Solve for \( V_C \):

\[ V_C = V_{CC} - I_C R_C \]

or

\[ V_C = V_{CE} + I_E R_E \]

Solve for \( V_B \):

\[ V_B = V_{CC} - I_B R_B \]

or

\[ V_B = V_{BE} + I_E R_E \]
### Voltage Divider Bias Example 1

- **$V_{CC}$ = 22V**
- **$R_1$ = 39k$\Omega$**
- **$R_2$ = 3.9k$\Omega$**
- **$R_C$ = 10k$\Omega$**
- **$R_E$ = 1.5k$\Omega$**
- **$\beta$ = 140**

### Voltage Divider Bias Example 2

- **$V_{CC}$ = 18V**
- **$R_1$ = 39k$\Omega$**
- **$R_2$ = 8.2k$\Omega$**
- **$R_C$ = 3.3k$\Omega$**
- **$R_E$ = 1k$\Omega$**
- **$\beta$ = 120**
Voltage Divider Bias Example 3

\[ V_{CC} = 16V \]
\[ R_1 = 62k\Omega \]
\[ R_2 = 9.1k\Omega \]
\[ R_C = 3.9k\Omega \]
\[ R_E = 0.68k\Omega \]
\[ \beta = 80 \]

Design of CE Amplifier with Voltage Divider Bias

1. Select a value for \( V_{CC} \)
2. Determine the value of \( \beta \) from spec sheet or family of curves
3. Select a value for \( I_CQ \)
4. Let \( V_{CE} = \frac{1}{2} V_{CC} \) (typical operation, \( 0.4 V_{CC} \leq V_C \leq 0.6 V_{CC} \))
5. Let \( V_E = 0.1 V_{CC} \) (for good operation, \( 0.1 V_{ce} \leq V_E \leq 0.2 V_{CC} \))
6. Calculate \( R_E \) and \( R_C \)
7. Let \( R_2 \leq 0.1 \beta R_E \) (for this calculation, use low value for \( \beta \))
8. Calculate \( R_I \)

\[ R_I = R_E \left( \frac{V_{CC} - V_B}{V_B} \right) \]
CE Amplifier Design

- Design a Common Emitter Amplifier with Voltage Divider Bias for the following parameters:
  - $V_{CC} = 24\text{V}$
  - $I_C = 5\text{mA}$
  - $V_E = 0.1V_{CC}$
  - $V_C = 0.55V_{CC}$
  - $\beta = 135$
CE Amplifier Design

Voltage Divider Bias

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Collector Feedback Bias

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BJT Biasing 4

For the Collector Feedback Bias Configuration:

- Draw Equivalent Input circuit
- Draw Equivalent Output circuit
- Write necessary KVL and KCL Equations
- Determine the Quiescent Operating Point
  - Graphical Solution using Loadlines
  - Computational Analysis
- Design and test design using a computer simulation
DC Bias with Collector (Voltage) Feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.
In this bias circuit the Q-point is only slightly dependent on the transistor $\beta$.

Base – Emitter Loop Solve for $I_B$

Applying Kirchoff’s voltage law: $-V_{CC} + I_c' R_C + I_B R_B + V_{BE} + I_c R_E = 0$

Note: $I_c' = I_c = I_B$

Since $I_e = (\beta + 1) I_B$ then: $-V_{CC} + (\beta + 1) I_B R_C + I_B R_B + V_{BE} (\beta + 1) I_B R_E = 0$

Simplifying and solving for $I_B$: $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)(R_C + R_E)}$
Applying Kirchoff's voltage law: 

\[-V_{CC} + I_E R_C + I_a R_B + V_{BE} + I_E R_E = 0\]

Since \( I_a = (\beta + 1) I_E \) then: 

\[-V_{CC} + I_E R_C + I_E \left( \frac{R_B}{(\beta + 1)} \right) + V_{BE} + I_E R_E = 0\]

Simplifying and solving for \( I_E \): 

\[I_E = \frac{V_{CC} - V_{BE}}{R_B + (R_C + R_E) \left( \frac{1}{(\beta + 1)} \right)}\]

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Applying Kirchoff's voltage law: 

\[I_E R_C + V_{CE} + I_E' R_C - V_{CC} = 0\]

Since \( I_E' = I_E \) and \( I_E = (\beta + 1) I_E \): 

\[I_E (R_C + R_E) + V_{CE} - V_{CC} = 0\]

Solving for \( V_{CE} \): 

\[V_{CE} = V_{CC} - I_E (R_E + R_C)\]
Network Example

Network Example

Voltage Divider Bias
Design of CE Amplifier with Collector Feedback Bias

1. Select a value for $V_{cc}$
2. Determine the value of $\beta$ from spec sheet or family of curves
3. Select a value for $I_{EQ}$
4. Let $V_{CE} = \frac{1}{2} V_{CC}$ (typical operation, $0.4 V_{CC} \leq V_C \leq 0.6 V_{CC}$)
5. Let $V_{E} = 0.1 V_{CC}$ (for good operation, $0.1 V_{CC} \leq V_E \leq 0.2 V_{CC}$)
6. Calculate $R_E$, $R_C$ and $R_B$

\[
\begin{align*}
V_E &= 0.1 V_{CC} \\
R_E &= \frac{1V_{CC}}{I_E} \\
R_C &= \frac{V_{CC} - V_{CQ}}{I_E} = \frac{V_{CC} - 0.6V_{CC}}{I_E} \\
R_B &= \frac{V_{CC} - I_E R_C - V_{BE} - I_E R_B}{I_E} \\
R_H &= \frac{V_{CC} - I_E (R_C + R_H) - 0.7V}{I_E} \\
\end{align*}
\]
Common Emitter Bias with Dual Supplies

Voltage Divider Bias with Dual Power Supply

![Diagram of voltage divider bias with dual power supply]
### Voltage Divider Bias with Dual Power Supply

#### Input Circuit

Find $V_{TH}$ and $R_{TH}$

$$V_{TH1} = V_{CC} \left( \frac{R_2}{R_1 + R_2} \right)$$

(Note $V_{EE}$ is negative)

$$V_{TH2} = -V_{EE} \left( \frac{R_1}{R_1 + R_2} \right)$$

$$V_{TH} = V_{TH1} + V_{TH2}$$

$$V_{TH} = V_{CC} \left( \frac{R_2}{R_1 + R_2} \right) - V_{EE} \left( \frac{R_1}{R_1 + R_2} \right)$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

#### Output Circuit

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E - V_{EE} = 0$$

If we assume $I_E \ll I_C$ (when $\beta > 100$)

$$I_C = \frac{V_{CC} + V_{EE} - V_{CE}}{R_C + R_E}$$

If we use the exact solution $I_C = \alpha I_E$

$$I_C = \frac{V_{CC} + V_{EE} - V_{CE}}{R_C + \frac{R_E}{\alpha}}$$

where $\alpha = \frac{\beta}{\beta + 1}$
Voltage Divider Bias with Dual Power Supply

PSpice Simulation
**PSpice Bias Point Simulation**

**PSpice Simulation for DC Bias**
The response of $V_C$ demonstrates that it reaches a peak value near the Q point and then decreases.

The response of $V_{CE}$ demonstrates that it rises rapidly towards the Q point and then increases gradually towards a maximum value.
PSpice Simulation for AC Sweep

![PSpice Simulation for AC Sweep](image1)

PSpice Simulation for AC Sweep

![PSpice Simulation for AC Sweep](image2)