

**OBJECTIVE**

A common application of the edge-triggered JK Flip-flop is in the construction of binary counters to count the number of events or time the duration of various events. Counters may also be used to divide the frequency of a clock. In this experiment, the student will design, build, and test synchronous and asynchronous counters.

**EQUIPMENT AND PARTS REQUIRED**

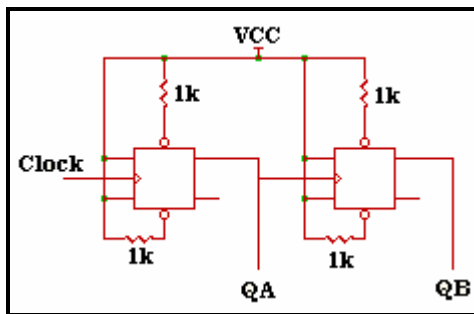
- 1 Protoboard
- AR 74LS08, 74LS76, 74LS393

**INTRODUCTION**

In the previous experiment, the edge-triggered JK Flip-flop was wired to operate as a toggle. Every time a clock pulse was detected at the input, the output changed state. After two clock pulses were detected, the output of the T Flip-flop returned to its original state. As a result, there were two state changes of the output and the frequency of the input clock was divided by two. Therefore two events occurred, the number of clock pulses were counted and the frequency of the output was divided by 2. The circuit of Figure 1 contains a truth table and logic diagram for a two bit asynchronous binary counter with Q<sub>B</sub> the MSB. The truth table of Figure 1 shows the counting action of this circuit. The frequency of the input clock is divided by two for the first FF and then divided by two again for the second FF. The frequency at Q<sub>B</sub> has been divided by four or 2<sup>n</sup> where n is the number of FFs in the circuit. There are also four states in the truth table. This factor 2<sup>n</sup> is also called the Modulus or MOD of the counter. Since this counter has 2 FFs, it is referred to as a MOD 4 counter. The MOD of any counter may be modified by connecting the proper combinational logic between the outputs of the appropriate FF and the Clear input. To convert the counter in Figure 1 to a MOD 3 counter, AND the Q<sub>A</sub> and Q<sub>B</sub> inputs and connect the output of the AND gate to the CLEAR input of all the FFs. If the input clock frequency and the MOD of a counter is known, the frequency at the output of the last FF may be calculated from the equation:

$$F_{OUT} = \frac{F_{CLOCK}}{MODULUS} \tag{1}$$

Figure 1 is an asynchronous device since the preceding FF must complete one cycle to provide the clock pulse for the next FF in the counter. The FFs do not change state at the same time and this creates a ripple effect in the way that the output of each FF changes state. This ripple effect is more noticeable in a MOD 16 or higher counter when the count resets from 15 or the maximum count back to 0. Another name for the asynchronous counter is the ripple counter.



CLOCK PULSE	Q <sub>B</sub>	Q <sub>A</sub>
0	0	0
1	0	1
2	1	0
3	1	1

**FIGURE 1**

Since some digital functions are performed in BCD, the decade counter is often used. To make a decade counter will require 4 FFs or a MOD 16 counter since three FFs would only give us a MOD 8 counter. To create an asynchronous decade counter, AND outputs Q<sub>D</sub> and Q<sub>B</sub> of the MOD 16 counter

## ELEC 241 Experiment 7 Synchronous And Asynchronous Counters

together and connect the output of the AND gate to the Clear inputs of every the FF. The output of the counter reaches 10 for a moment before the output of the AND gate resets the counter to 0. This short time that the counter has an output of 10 may be observed on the  $Q_B$  output as a glitch. When the output of a counter is designed to have a sequence of states less than the maximum modulus, the counter is said to have a truncated sequence.

The circuit of Figure 1 is an asynchronous device because the FFs do not change states at the same time. Assume that each FF has a propagation delay time of 10 ns.

There will be delay between the time each of the FFs input and output changes. For a MOD 16 counter, there are 4 FFs so the total propagation delay for the counter between the input clock pulse and the output state change of  $Q_D$  is 40 ns.

### PROCEDURE

1. Design and build an MOD 16 asynchronous counter using the 74LS76, and other IC's as necessary. Connect the Clock input to a debounced switch or a 1HZ TTL level pulse input. Connect the  $Q_A$  to  $Q_D$  outputs of the counter to the monitor LED's on the protoboard. Monitor the outputs and construct the state table and draw the waveform diagram.
2. Repeat step 1 for a MOD 16 synchronous counter.
3. Design a MOD 10 asynchronous counter using the 74LS393 and any additional IC's as necessary. Create a state table predicting the outputs. Using PSpice, draw the schematic diagram and run Time Domain (Transient) analysis and display the outputs Clock,  $Q_D$ ,  $Q_C$ ,  $Q_B$ , and  $Q_A$  in that order. Print the schematic and Probe output. To the predicted state table, add the outputs observed from Probe and compare the two. On the Probe output, identify if a glitch occurs in the count transition from 1001 to 0000.

### QUESTIONS

1. How many flip-flops are required for a MOD 100 counter?
2. Draw the logic diagram of a MOD 11 counter using a 74LS93A
3. Design a MOD 16 synchronous up/down counter. Draw the truth table and waveform diagram for this counter for both the up and down sequence.